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EXAMINER	
PEIKARI, BEHZAD	
ART UNIT	**PAPER NUMBER**
2189	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/27/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/674,981	ELLIS ET AL.	
	Examiner	Art Unit	
	B. James Peikari	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 October 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The previous objections to the drawings are withdrawn due to the corrected drawings filed on October 2, 2006.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5-11, 13-18 and 20-31 are rejected under 35 U.S.C. 102(b) as being anticipated by Leung (US Pub No 2001/0008496).

(A) As per claim 1, Leung discloses a memory device comprising:

a storage array comprised of a plurality of memory cells organized into an array of rows (Fig 2, Ref 201) ;

an interface buffer coupled to the storage array, and having a first interface to couple the memory device to a first memory bus to couple the memory device to an external memory controller (Fig 2, Ref 208); and

refresh logic associated with the interface buffer to detect a pattern on the memory bus to carry out a refresh operation on a row within the storage array during a

period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array (note Fig 2, Ref 207, wherein the pattern to be detected is taught by a particular number of consecutive idle cycles in Leung).

(B) As per claim 2, Leung discloses the memory device of claim 1, wherein the refresh logic is a component of the interface buffer, and wherein the memory device is comprised of a circuit board to which is attached at least one integrated circuit that comprises the storage array and at least one integrated circuit that comprises the interface buffer [Note that Fig 2 is a memory block of Fig 1. The interface buffer is interpreted to be everything other than the memory array, thus the refresh logic is a component of the interface buffer (Fig 2)].

(C) As per claim 3, Leung discloses the memory device of claim 1, wherein the first memory bus provides a point-to-point connection between the memory device and the external memory controller, the interface buffer has a second interface to couple the memory device to a second memory bus to provide a point-to-point connection between the memory device and another memory device, and the interface buffer passes through bus activity between the first and second memory busses that does not involve the storage array (Page 12, Paragraph 123).

(D) As per claim 5, the memory device of claim 3, wherein the refresh logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the storage array, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on a

row within the storage array without delaying the carrying out of an access command involving the storage array (Paragraph 10).

(E) As per claim 6, the memory device of claim 5, wherein the refresh logic carries out a refresh operation on a row within the storage array during a period of time in which a transaction between the external memory controller and the other memory device occurs [The storage array is idle during the time a controller performs a transaction with a different memory device, thus a refresh operation can occur (Paragraph 14)].

(F) As per claim 7, the memory device of claim 3, wherein the refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller, providing an opportunity for the refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array (Paragraph 12).

(G) As per claim 8, the memory device of claim 3, wherein the refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array [Powering down of the memory bus is interpreted as the memory bus being idle, since less power is required when transmitting than when not transmitting (Paragraph 12)].

(H) As per claim 9, an interface buffer comprising:

a local interface to a storage array comprised of a plurality of memory cells organized into an array of rows (Fig 2, Ref 201);

a first interface to couple the storage array to a first memory bus to couple the storage array to an external memory controller wherein the first memory bus provides a point-to-point connection between the first interface and the external memory controller (Fig 2, Ref 208);

a second interface to couple the storage array to a second memory bus to couple the second interface to another interface buffer to couple another storage array to the external memory controller through the interface buffer wherein the second memory bus provides a point-to-point connection between the second interface and the other interface buffer [In a serial system disclosed in Paragraph 123, a similar interface exists (Fig 2, Ref 208); and

refresh logic to to monitor (i.e., detect) idle cycles to carry out a refresh operation on a row within the storage array during a period of time in which there are no transactions carried out by the external memory controller on the first memory bus that involve the storage array (Fig 2, Ref 207).

(l) As per claim 10, the interface buffer of claim 9, wherein the interface buffer is comprised of at least one integrated circuit, the storage array is comprised of at least one integrated circuit, and both the at least one integrated circuit comprising the interface buffer and the at least one integrated circuit comprising the storage array are attached to a circuitboard to comprise a memory device [Note that Fig 2 is a memory block of Fig 1. The interface buffer is interpreted to be everything other than the memory

array, thus the refresh logic is a component of the interface buffer (Fig 2), (Paragraph 25)].

(J) As per claim 11, the interface buffer of claim 10, wherein the first interface is coupled to the first memory bus and the second interface is coupled to the second memory bus when the memory device is coupled to another circuitboard to which the external memory controller is attached [The first interface must be coupled to the first memory bus and the second interface coupled to the second memory bus in order to properly control the devices, Fig 1 discloses a memory controller separate from the memory block devices (Fig 1, Ref 120)].

(K) As per claim 13, the memory device of claim 9, wherein the refresh logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the storage array, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array (Paragraph 10).

(L) As per claim 14, the memory device of claim 13, wherein the refresh logic carries out a refresh operation on a row within the storage array during a period of time in which a transaction between the external memory controller and the other storage array occurs [The storage array is idle during the time a controller performs a transaction with a different memory device, thus a refresh operation can occur (Paragraph 14)].

(M) As per claim 15, the memory device of claim 9, wherein the refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the storage array will be transmitted by the external memory controller, providing an opportunity for the refresh logic to carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array (Paragraph 12).

(N) As per claim 16, the memory device of claim 9, wherein the refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the refresh logic to opportunistically carry out a refresh operation on a row within the storage array without delaying the carrying out of an access command involving the storage array [Powering down of the memory bus is interpreted as the memory bus being idle, since less power is required when transmitting than when not transmitting (Paragraph 12)].

(O) As per claim 17, a memory system comprising:

a memory controller (Fig 1, Ref 120);

a first memory bus coupled to the memory controller (Fig 1);

a first memory device having a first storage array comprised of a plurality of memory cells organized into rows (Fig 2, Ref 201) and a first interface buffer coupled within the first memory device to the first storage array, wherein the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface (Fig 2, Ref 208), a second interface, and a first refresh logic to carry out a

refresh operation on a row within the first storage array during a period of time in which there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array (Fig 2, Ref 207);

a second memory bus coupled to the second interface (Paragraph 123, Fig 1, Ref 101); and

a second memory device having a second storage array comprised of a plurality of memory cells organized into rows (Fig 2, Ref 201) and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the third interface and the second interface (Fig 2, Ref 208), and a second refresh logic to monitor (i.e., detect) idle cycles to carry out a refresh operation on a row within the second storage array during a period of time in which there are no transactions carried out by the memory controller on the second memory bus that involve the second storage array (Fig 2, Ref 207).

(P) As per claim 18, the memory system of claim 17, wherein the first interface buffer passes through bus activity between the first and second memory busses that does not involve the first storage array (Paragraph 123).

(Q) As per claim 20, the memory system of claim 17, wherein the first refresh logic monitors activity on the first memory bus to identify a dead time in which no commands are received from the first memory bus involving the first storage array, providing an opportunity for the first refresh logic to opportunistically carry out a refresh

operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array (Paragraph 10).

(R) As per claim 21, the memory system of claim 20, wherein the first refresh logic carries out a refresh operation on a row within the first storage array during a period of time in which a transaction between the memory controller and the second storage array occurs [The storage array is idle during the time a controller performs a transaction with a different memory device, thus a refresh operation can occur (Paragraph 14)].

(S) As per claim 22, the memory system of claim 20, wherein the second refresh logic monitors activity on the second memory bus to identify a dead time in which no commands are received from the second memory bus involving the second storage array, providing an opportunity for the second refresh logic to opportunistically carry out a refresh operation on a row within the second storage array in parallel with the first refresh logic carrying out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the second storage array (Paragraph 10).

(T) As per claim 23, the memory system of claim 17, wherein the first refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the first storage array will be transmitted by the memory controller, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array (Paragraph 12).

(U) As per claim 24, the memory system of claim 23, wherein the second refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the second storage array will be transmitted by the memory controller, providing an opportunity for the second refresh logic to carry out a refresh operation on a row within the second storage array in parallel with the second refresh logic carrying out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the second storage array (Paragraph 12).

(V) As per claim 25, the memory system of claim 17, wherein the first refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the first refresh logic to opportunistically carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array [Powering down of the memory bus is interpreted as the memory bus being idle, since less power is required when transmitting than when not transmitting (Paragraph 12)].

(W) As per claim 26, the memory system of claim 25, wherein the first refresh logic monitors the second memory bus for the occurrence of a powering down of the second memory bus, providing an opportunity for the second refresh logic to opportunistically carry out a refresh operation on a row within the second storage array in parallel with the second refresh logic carrying out a refresh operation on a row within the second storage array without delaying the carrying out of an access command involving the second storage array (Paragraph 23, 25).

(X) As per claim 27, a computer system comprising:

a processor (Paragraph 48);

a disk storage device coupled to the processor (It is well known in the art that a computer system can have a disk storage)

a memory controller coupled to the processor (Fig 1, Ref 120);

a first memory bus coupled to the memory controller (Fig 1);

a first memory device having a first storage array comprised of a plurality of memory cells organized into rows (Fig 2, Ref 201) and a first interface buffer coupled within the first memory device to the first storage array, wherein the first interface buffer provides a first interface by which the first memory device is coupled to the first memory bus forming a point-to-point connection between the memory controller and the first interface (Fig 2, Ref 208), a second interface, and a first refresh logic to carry out a refresh operation on a row within the first storage array during a period of time in which there are no transactions carried out by the memory controller on the first memory bus that involve the first storage array (Fig 2, Ref 207);

a second memory bus coupled to the second interface (Paragraph 123, Fig 1, Ref 101); and

a second memory device having a second storage array comprised of a plurality of memory cells organized into rows (Fig 2, Ref 201) and a second interface buffer coupled within the second memory device to the second storage array, wherein the second interface buffer provides a third interface by which the second memory device is coupled to the second memory bus forming a point-to-point connection between the

third interface and the second interface (Fig 2, Ref 208), and a second refresh logic to monitor (i.e., detect) idle cycles to carry out a refresh operation on a row within the second storage array during a period of time in which there are no transactions carried out by the memory controller on the second memory bus that involve the second storage array (Fig 2, Ref 207).

(Y) As per claim 28, the computer system of claim 27, wherein the first refresh logic carries out a refresh operation on a row within the first storage array during a period of time in which a transaction between the memory controller and the second storage array occurs [The storage array is idle during the time a controller performs a transaction with a different memory device, thus a refresh operation can occur (Paragraph 14)].

(Z) As per claim 29, the computer system of claim 27, wherein the first refresh logic awaits a signal from the external memory controller to identify a dead time in which no commands involving the first storage array will be transmitted by the memory controller, providing an opportunity for the first refresh logic to carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array (Paragraph 10).

(AA) As per claim 30, the computer system of claim 29, wherein the memory controller is further comprised of a control register programmable by the processor to enable the transmitting of a signal by the memory controller to the first refresh logic to identify a dead time [The processor is coupled to the memory controller and processes

all reads and writes, thus it enables the transmitting of a signal by the memory controller to the first refresh logic to identify a dead time(Paragraph 10)].

(BB) As per claim 31, the computer system of claim 27, wherein the first refresh logic monitors the first memory bus for the occurrence of a powering down of the first memory bus, providing an opportunity for the first refresh logic to opportunistically carry out a refresh operation on a row within the first storage array without delaying the carrying out of an access command involving the first storage array [Powering down of the memory bus is interpreted as the memory bus being idle, since less power is required when transmitting than when not transmitting (Paragraph 12)].

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 4, 12 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leung as applied to claims 3, 9 and 18 above, and further in view of Curtis (US Patent 6,925,086).

(A) As per claim 4, Leung discloses the memory device of claim 3. Leung does not disclose using packets in the method wherein both a transfer of data between the external memory controller and the first interface of the interface buffer and a transfer of data between the second interface of the interface buffer and the other memory device occur with data transmitted in a packets. Curtis discloses using packets in a memory system (Col 1, Lines 46-60).

(B) As per claims 12 and 19, please see rejection of claim 4 above, claim 12 is rejected for similar reasons.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to incorporate the packet memory system of Curtis into the system of Leung, since this would have allowed for reduced memory latency (note Curtis, Col 1, Lines 33-35).

Response to Amendment

6. The remarks filed on October 30, 2006 have been carefully considered by the examiner but is not believed to put the application in condition for allowance.

(A) Regarding the rejections under 35 U.S.C. § 102(b), applicant disputes the examiner's interpretation of the scope of "pattern", as set forth in the Advisory Action

mailed on October 19, 2006. Applicant further cites a dictionary for extrinsic evidence of the meaning of "pattern". However, applicant's remarks are not commensurate in scope with the claims. The invention includes no limitation whatsoever on the scope of "pattern", other than its context within the claims. Therefore, a particular number of consecutive idle cycles falls well within the scope of "pattern", as claimed.

Any intended limitation of the scope of "pattern" should be included in the language of the claims.

(B) Regarding the rejections under 35 U.S.C. § 103(a), applicant's remarks set forth three criteria necessary to establish a *prima facie* case of obviousness, but do not include any further discussion of such criteria. Instead, the remarks indicate that dependent claims 4, 12 and 19 should be allowed because independent claims 1, 9 and 17 should be allowed. Consequently, claims 4, 12 and 19 are deemed to stand or fall with claims 1, 9 and 17, respectively.

Conclusion

7. This is an RCE of applicant's earlier Application No. 10/674,981. All claims are drawn to the same invention claimed in the earlier application and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the earlier application. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action in this case. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no, however, event will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James Peikari whose telephone number is (571) 272-4185. The examiner is generally available between 7:00 am and 7:30 pm, EST, Monday through Wednesday, and between 5:30 am and 4:00 pm on Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached at (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic

Business Center at 866-217-9197 (toll-free).

B. James Peikari
Primary Examiner
Art Unit 2189
12/24/06